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(54) Title of Invention: Production Method of Packaging for Semiconductor Equipment

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Detailed Descriptions:

1. Title of Invention:

Production Method of Packaging for Semiconductor Equipment

2. Scope of Patent Claims:

The production method of packaging for semiconductor equipment, which is characterized as being equipped with semiconductor equipment on the substrate that is composed of such a material that is possible for a selective etching, tying up the connecting wire with the above-mentioned semiconductor equipment as well as putting together the external electrode parts of the connecting wire with the extreme end of the external electrode parts of the above-mentioned substrate, and resin molding all together the above-mentioned connecting wires on the above-mentioned substrate, as well as removing etching from the above-mentioned substrate in the last stage.

3. Detailed Descriptions of Invention:

Areas of Industrial Applications:

This invention is in regard to the production method of packaging for semiconductor

equipment.

The background technologies and their problems:

Conventionally, the so-called chip-carrier type packaging has been used widely as one of the methods for producing packaging on the printed substrate with high accuracy. This method is of a lead-less type packaging method, through which an electrode, which is being extended to the rear surface of the packaging, is connected directly to the conductor pattern on the printed substrate by soldering.

There are two (2) types of methods in this chip-carrier type packaging, namely, a ceramic type method and plastic type method. However, not only that the packaging made by the ceramic type method is expensive, but also it has such a disadvantage that a cracking and/or peeling might occur at the connections between the ceramics and above-mentioned soldering parts and/or the conductors, due to the

differences of their coefficient of thermal expansion during the temperature cycle, when soldered directly to the printed substrate. On the other hand, however, although the packaging by the plastic type method is less expensive, it also has such disadvantages that a heat dissipation capacity is being poor, as well as the shape itself is not suitable for the automation of the packaging.

In Fig. 1, the construction of this conventional plastic type chip-carrier packaging is shown. This packaging (1) is produced in such a way that by dropping a liquid epoxy resin from the above, onto the parts, after having connected both ends of the chip (4) and electrode (2) through a wire bonding method with small size wires (5) of Au, after setting the chip (4), which is

consisting of the semiconductor equipment, onto the printed substrate (3), on which the electrode (2) of copper film is being formed in advance.

At this packaging (1), the resin layer (6) and printed substrate (3) surround the chip (4). Since the heat resistance of these resin layer (6) and printed substrate (3) is relatively higher, the heat that is generated by the chip (4) while it is working cannot be removed effectively towards outside of the packaging (1). That is to say that, the heat dissipation characteristic of the packaging (1) is poor, and it is one of the disadvantages of this particular component. Moreover, when the liquid resin epoxy is dropped onto the parts from above, as mentioned previously, it is pretty difficult to control the small specific amount of liquid dropping at a higher speed with a constant manner, thus making it very difficult to handle the packaging (1) with an automated mode.

On the other hand, there is a packaging that is called as a tape-carrier type packaging, which is different from the chip-carrier type packaging. Compared with the conventional type of chip-carrier type packaging, this type of packaging has such an advantage that the unit can be made much smaller. However, it also has some other disadvantages as such that, the heat dissipation characteristic is poor, as the chip is totally covered by the resin layer, as well as it requires a special equipment as being employed with a tape.

The Objective of the Invention:

The objective of this invention is that, to provide a production method of packaging for semiconductor equipment, which has a high heat dissipation capacity as well as with more reliable capabilities, so that the above-mentioned conventional problems can possibly be solved.

The Outline of the Invention:

The production method of packaging for semiconductor equipment, which is related to this

invention is characterized as being equipped with semiconductor equipment on the substrate that is composed of such a material that is possible for a selective etching, tying up the connecting wire with the above-mentioned semiconductor equipment, as well as putting together the external electrode parts of the connecting wires with the extreme end of the external electrode parts of the above-mentioned substrate, and resin molding all together with the above-mentioned connecting wires on the above-mentioned substrate, as well as removing etching from the above-mentioned substrate in the last stage. By doing it this way, it is possible that to produce the lead-less type packaging for semiconductor equipment, which has a high heat dissipation capacity as well as with more reliable capabilities, through an automated, simple, and less expensive way. The external electrode parts, which are mentioned above may be represented by the above-mentioned connecting wires, and/or may be separated from the above-mentioned connecting wires, and be connected to the above-mentioned connecting wires.

Implemented Examples:

In the following, the production method of packaging for semiconductor equipment, which is related to this invention is described by using some sketched diagrams based on the implemented examples.

Fig. 2A ~ 2D are showing the process diagrams to explain the production method of packaging for semiconductor equipment, which is related to this invention by using No. 1 Implemented Example. In the following, the process is explained starting from Fig. 2A and in order.

First of all, in Fig. 2A, the Au layer (12) of thickness 1 [μ], Ni layer (13) of thickness 1 [μ], and Au layer (14) of thickness 3 [μ] are plated on top of the substrate (11) of Fe in order, and installed the chip connection part (16) and external electrode parts (17) (18), which are consisting of the chip (15) for the semiconductor equipment, onto the specific locations of the chip connection

part (11g) and external electrode connection parts (11h) (11i) on the above-mentioned substrate (11), respectively.

In Fig. 3, the plan view of the above-mentioned substrate (11), on which the process that is shown in Fig. 2A has been completed, is shown. Next, in Fig. 2B, after having installed the chip (15) onto the above-mentioned chip connection part (16), connect the chip (15) and above-mentioned external electrode parts (17) (18) with the wire (19), which are composed of Au small wires, respectively, by means of the wire bonding method. Next, in Fig. 2C, in order to integrate the above-mentioned external electrode parts (17) (18), which are being installed on the substrate (11) that is shown in Fig. 2B, chip connection part (16), chip (15), and wire (19), establish the resin molding layer (20), which is composed of an epoxy, onto the above-mentioned substrate (11) by means of the well-known transfer-molding method. In this implemented example, the thickness "t" of the above-mentioned resin molding layer (20) has been set to 1 [mm].

Next, in Fig. 2C, only the Fe is etched selectively, however, the resin molding layer (20) and Au layer (12) are not etched practically by spray-etching from the back side (11a) of substrate (11) with such a solution like a ferric chloride ($FeCl_3$) for example, by which the etching can be avoided, so that the above-mentioned substrate (11) is removed, and that the lead-less type packaging (21) that is shown in Fig. 2D can be completed. Among the bottom surfaces of the Au layer (12), which were exposed by the previous etching, the external electrode parts (17) (18) at the bottom surface of the Au layer (12) turn out to be the external electrode surfaces (12b) (12c), and the bottom surface of the Au layer (12) at the chip connection part (16) turns out to be the

heat dissipation surface (12a).

When installing the packaging (21), which was completed throughout he above-mentioned process, onto the printed substrate, the above-mentioned external electrode surfaces (12b) (12c) that are shown in Fig. 2D can be connected directly to the conductor patterns on the printed substrate by soldering.

The above-mentioned heat dissipation surface (12a) in No. 1 Implemented Example turns out to be a heat dissipation surface for the heat that is generated by the chip (15) while it is working. Since the heat conductivity of a metal is extremely high, the heat that is generated by the chip (15) flows very quickly towards outside alongside the chip connection part (16), which is made of a metal, and removed effectively through the heat dissipation surface (12a). However, in order to remove the heat that is generated by the chip (15) more effectively, it is desirable that a part of the heat dissipation fins, which all together possess a broad surface area, is pushed to the above-mentioned heat dissipation surface (12a), so that the heat is removed through air cooling.

Since the packaging (21), which is explained in No. 1 Implemented Example, can be produced by such a simple process that is shown in Fig. 2A ~ 2D, the equipment which is being used for the conventional method can be utilized throughout the entire process. No only that, those special equipment which was mentioned previously and required for producing the chip-carrier type packaging is needed at here. Therefore, it is possible that to produce the lead-less type packaging (21) for semiconductor equipment, which has a high heat dissipation capacity as well as with more reliable capabilities, through an automated, simple, and less expensive ways. Moreover, in the above-mentioned No. Implemented Example, the transfer-molding method is employed as the method of forming the resin molding layer (20). This transfer-molding method will provide such an advantage that not only producing a reliable resin molding material, but also makes it possible

to produce the packaging in an automated manner, based on its easy molding automation and mass-production features.

In the above-mentioned No. 1 Implemented Example, just like the case that is shown in Fig. 2A, by slightly etching the upper surface of the substrate (11) with the previously mentioned $FeCl_3$ solution after having installed the chip connection part (16) and external electrode parts (17) (18), the undercut parts (11a) ~ (11f) can be formed on the substrate (11), which is under the chip connection part (16) and external electrode parts (17) (18), as shown in Fig. 4A, and the packaging (21) that is shown in Fig. 4B can be completed in the same method as shown in Fig. 2B ~ 2D. In this way, since the above-mentioned undercut parts (11a) ~ (11f) can be formed at the bottom of the chip connection part (16) and external electrode parts (17) (18) by means of the etching, which was described previously, the protruded parts (20a) ~ (20f) can be formed with the resins filling up the parts. Therefore, the above-mentioned chip connection part (16) and external electrode parts (17) (18) are supported by these protruded parts (20a) ~ (20f) from the bottom subsequently, and that the chip connection part (16) and external electrode parts (17) (18) can be prevented from falling off from the resin-molding layer (20) while the packaging (21) is used.

Tokugansho 59-208756 (4)

Moreover, as the chip connection part (16) and external electrode parts (17) (18) are formed in such a way that not being protruded from the bottom surface of the resin molding layer (20), both of these chip connection part (16) and external electrode parts (17) (18) can be protected further.

Fig. 5A ~ 5C are showing the process diagrams to explain the production method of packaging for semiconductor equipment, which is related to this invention by using No. 2 Implemented Example. In the following, the process is explained starting from Fig. 5A and in order.

First of all, in Fig. 5A, after having sprayed the well-known photo-resist on to the top surface of the substrate (11), which is 35 [μ] thick and made of Cu, execute the specific patterning. Next, by using such a solution like a ferric chloride ($FeCl_3$) that is previously mentioned for example, and by which only the Cu can be selectively etched, the surface of the above-mentioned substrate (11) is slightly etched, so that the chip connecting part (11g) and external electrode connecting parts (11h) (11i) can be formed individually on the surface of the above-mentioned substrate (11). And, after having removed the above-mentioned photo-resist, connect the chip (15) to the above-mentioned chip connecting part (11g) through the soldering layer (23), just as it was done in Fig. 5B for No.1 Implemented Example, and connect the chip (15) and above-mentioned external electrode parts (11h) (11i) with the wire (19), which are composed of Au small wires, respectively, by means of the wire bonding method. In this implemented example, however, a larger diameter of wire than the one that was used for No. 1 Implemented Example was used, due to the reasons that would be explained later in this report. Next, establish the resin molding layer (20) on the above-mentioned substrate (11), just as the same way that was done for No. 1 Implemented Example. And, next complete the packaging (24) by removing the etching on the above-mentioned substrate (11), just as the same way that was done for No. 1 Implemented Example. The end part of wire (19), which was exposed by the previous etching turns out to be the external electrode parts (17) (18), and the bottom surface of the soldering layer (24) turns out to be the heat dissipation surface (23a).

When installing the packaging (24), which was completed throughout he above-mentioned process, onto the printed substrate, the above-mentioned external electrode parts (17) (18) that are shown in Fig. 5D can be connected directly to the conductor patterns on the printed substrate by soldering, the same way that was used for No. 1 Implemented Example. As it is clear now by

the above reasons, since the ends of the wire (19) are used as the external electrode parts (17) (18) in this implemented example, it is desirable to use the larger diameter of wire (19) as it was mentioned previously. The function of the heat dissipation surface (23a) is the same as it was for No. 1 Implemented Example.

The packaging (24) for the above-mentioned No. 2 Implemented Example is a little different from the packaging (21) for No. 1 Implemented Example, and the external electrode connection parts (11h) (11i), which were installed during the photo-resist and etching processes, are being connected directly to the wire (19), thus requiring no formations of the Au layer (12)(14) and Ni layer (13) that had been established for the packaging of No. 1 Implemented Example. The photo-resist and etching processes for the above case is much simpler compared with the plating process that was used for the packaging (21) for No. 1 Implemented Example. Also, by implementing this photo-resist and etching processes, the usage of such a precious metal like Au is going to be eliminated.

In the above-mentioned No. 1 and No. 2 Implemented Examples, it was mentioned with regard to a single chip to be installed at the single chip connection part and resin molding. However, based on this prototype idea, it is also possible to produce multiple numbers of packaging, all of which will have a single chip individually, at the same time, by installing multiple numbers of chip connection parts on a substrate, attaching multiple numbers of chips individually, resin molding in an integrated manner, and finally cut into the pieces. Furthermore, after having installed various kinds of chips and passive devices such as, condenser and resisters onto the substrate, and resin molding integrally, it is possible to produce the packaging that will have a various kind of functions, as well as the ones with highly integrated circuit element.

As the materials for the substrate for the above-mentioned No. 1 Implemented Example, it may

be another type of metal, such as Cu and the like, as long as the selective etching is possible, and by the same token, the materials for the substrate for the above-mentioned No. 2 Implemented Example, it may be some other type of metal, such as Fe and the like. Moreover, in the case of No. 1 Implemented Example, some other type of materials such as, polymidamide type resin can be used as well. In this case,

however, a mixture of hydrazine and ethylenediamine can be used as the etching liquid that was mentioned previously.

Effect of the Invention:

By the production method of packaging for semiconductor equipment, which is related to this invention, it is possible to produce the small size of packaging, which has a high heat dissipation capacity for the heat that is generated by the semiconductor equipment at the time of operation, as well as with more reliable capabilities, through an automated, relatively simple, and less expensive way.

4. Brief Descriptions for Sketched Diagrams

Fig. 1 shows the sectional view of chip-carrier type packaging construction of the conventional plastic type, and Fig. 2A ~ 2D are showing the process diagrams to explain the production method of packaging for semiconductor equipment, which is related to this invention by using No. 1 Implemented Example. Fig. 3 shows the plan view of substrate on which the process that is shown in Fig. 2A has been completed, and Fig. 4A and 4E are showing the similar views as the previous Fig. 2A ~ 2D, which are showing the deformed example of above-mentioned No. 1 Implemented Example. Fig. 5A ~ 5C are showing the process diagrams to explain the production

method of packaging for semiconductor equipment, which is related to this invention by using No. 2 Implemented Example.

And, in these diagrams, the following Item Numbers are representing;

(1), (21), (22), and (24) ---------- Packaging

(2), and (15) ---------- Chip

(3), and (19) ---------- Wire

(11) ---------- Substrate

(11h), and (11i) ---------- External Electrode Connection Parts

(17), and (18) ---------- External Electrode Part

(20) ---------- Resin Molding Layer

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Fig. 1

Fig. 2A

Fig. 2B

Fig. 2C

Fig. 2D

Fig. 3

Fig. 4A

Fig. 4B

Fig. 5A

Fig. 5B

Fig. 5C

AFFIDAVIT

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⑭半導体装置のパッケージの製造方法

⑳特　　願　昭58—83188

㉒出　　願　昭58(1983)5月12日

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明　細　書

1. 発明の名称

半導体装置のパッケージの製造方法

2. 特許請求の範囲

選択エッチング可能な材料から成る基板上に半導体装置を載置し、接続用ワイヤを上記半導体装置に接続すると共にこの接続用ワイヤの外部電極部を上記基板の外部電極接続部位に接続し、次いで上記基板上において上記半導体装置及び上記接続用ワイヤを一体に樹脂モールドし、しかる後上記基板をエッチング除去することを特徴とする半導体装置のパッケージの製造方法。

3. 発明の詳細な説明

産業上の利用分野

本発明は、半導体装置のパッケージの製造方法に関する。

従来技術とその問題点

従来、プリント基板上の実装密度の高いパッケージとして、チップキャリアタイプのパッケージが知られている。このパッケージはリードレスタイプのパッケージで、パッケージの底面に引き出されているハンダ付け可能な電極をプリント基板の導体パターンに直接ハンダ付けして接続することにより実装を行うものである。

このチップキャリアタイプパッケージには、セラミックタイプとプラスチックタイプとがある。セラミックタイプはパッケージ自体が高価であるばかりでなく、プリント基板に直接ハンダ付けすると、実使サイクル時にセラミックと上記ハンダ及び上記導体との間の熱膨張係数の差によって接続部にはがれやクラックが生じる恐れがあるという欠点を有している。一方、プラスチックタイプはパッケージが安価であるという利点を有しているが、耐湿性が悪く、また形状がパッケージの製造の自動化に適していないという欠点を有している。

このような従来のプラスチックタイプのチップキャリアタイプパッケージの構造を第1図に示す。このパッケージ(1)は、銅箔製の電極(2)が予め形成されているプリント基板(3)上に半導体装置を搭載

するチップ(4)を載置し、ワイヤボンディング法により上記チップ(4)と上記電極(2)の一端とをAuの細線から成るワイヤ(5)で接続した後、上方より板状のエポキシ樹脂を載下させて硬化成形することによつて作る。

このパッケージ(1)において、チップ(4)は樹脂層(6)とプリント基板(3)とによつて囲まれている。これらの樹脂層(6)及びプリント基板(3)の熱抵抗は共に大きいので、その動作時においてチップ(4)で発生する熱をパッケージ(1)の外部に効果的に放散することができない。即ち、このパッケージ(1)は放熱性が悪いという欠点を有している。また上記の板状のエポキシ樹脂を載下する際に、低温の樹脂を一定量、しかも高速で載下することが難しく、このためにパッケージ(1)はパッケージの製造の自動化に適していないという欠点を有している。

一方、上述のチップキャリアタイプパッケージとは異なるパッケージにテープキャリアタイプパッケージがある。このタイプのパッケージは従来のチップキャリアタイプパッケージよりもさらに小形化できるという利点を有するが、チップが樹脂層によつて完全に覆われているため熱放散性が良好でないこと、テープを用いているために特殊な装置が必要である等の欠点を有している。

発明の目的

本発明は、上述の問題にかんがみ、熱放散性が良好でかつ信頼性の高い半導体装置のパッケージの製造方法を提供することを目的とする。

発明の概要

本発明に係る半導体装置のパッケージの製造方法は、選択エッチング可能な材料から成る基板上に半導体素子を載置し、接続用ワイヤを上記半導体素子に接続すると共にこの接続用ワイヤの外部電極部側を上記基板の外部電極接続部位に接続し、次いで上記基板上において上記半導体素子及び上記接続用ワイヤを一体に樹脂モールドし、しかる後上記基板をエッチング除去するようにしている。このようにすることによつて、熱放散性が良好でかつ信頼性の高いリードレスタイプのパッケージを、簡便かつ安価な方法によつて自動的に製造することができる。なお上記外部電極部は上記接続用ワイヤ自体が兼ねていてもよいし、上記接続用ワイヤとは別に設けられかつ上記接続用ワイヤが接続されているものでもよい。

実施例

以下本発明に係る半導体装置のパッケージの製造方法の実施例につき図面を参照しながら説明する。

第2A図～第2D図は本発明の第1実施例による半導体装置のパッケージの製造方法を説明するための工程図である。以下第2A図から工程順に説明する。

まず第2A図において、厚さ5〔μ〕のFe板の基板(11)の上に、厚さ1〔μ〕のAu層(12)、厚さ1〔μ〕のNi層(13)及び厚さ3〔μ〕のAu層(14)をめつきして、半導体素子を搭載するチップ(15)の搭載部(11a)及び外部電極部(11b)(11c)のそれぞれを上記基板(11)の所定のチップ載置部位(11e)及び外部電極接続部位(11f)(11g)のそれぞれに設ける。第2A図に示す工程終了後の上記基板(11)の平面図を第3図に示す。次に第2B図において、上記チップ載置部(11a)にチップ(15)を載置した後、ワイヤボンディング法によつてこのチップ(15)と上記外部電極部(11b)(11c)とをそれぞれAuの細線から成るワイヤ(16)で接続する。次に第2C図において、第2B図の基板(11)の上に設けられた上記外部電極部(11b)(11c)、チップ載置部(11a)、チップ(15)及びワイヤ(16)を一体とするために、公知のトランスファ・モールド法（樹脂成形法）を用いて、エポキシから成る樹脂モールド層(17)を上記基板(11)上に形成する。なお本実施例においては、上記樹脂モールド層(17)の厚さtを1〔mm〕とした。

次に第2C図において、Feのみを選択的にエッチングするが樹脂モールド層(17)及びAu層(12)はエッチングしないエッチング液、例えば塩化第二鉄（$FeCl_3$）溶液を用いて、基板(11)の裏面(11h)側からスプレーエッチングすることにより、上記基板(11)を除去して、第2D図に示すリードレスタイプのパッケージ(21)を完成させる。上記エッチングによつて露出されたAu層(12)の下面のうち外部

電極部(17)(18)のAu層(13)の下面が外部電極面(12b)(12c)となり、またチップ収容部(19)のAu層(13)の下面が熱放散面(12a)となる。

上述のようにして完成されたパッケージ(10)をプリント基板上に実装する場合には、第2D図に示す上記外部電極面(12b)(12c)をプリント基板上の導体パターンに直接ハンダ付けして接続すればよい。

上述の第1実施例の熱放散面(12a)は、その動作時においてチップ(14)から発生する熱の放散面となつている。金属の熱伝導度は非常に高いので、チップ(14)から発生する熱は金属製のチップ収容部(19)を外方に向かつて迅速に流れて、熱放散面(12a)から放散されることによつて効果的に除去される。しかし、より効果的にチップ(14)の発生熱を除去するためには、広い表面積を有する放熱フインの一部を上記熱放散面(12a)に押し当てて空冷により熱を放散させるのが好ましい。

上述の第1実施例のパッケージ(10)は第2A図～第2D図に示すような簡単な工程によつて作ることができるばかりでなく、全ての製造工程に従来から用いられている装置を用いることができるので、テープキャリアタイプのパッケージにおいて必要な従来の特殊な装置が不要である。従つて、低価かつ安価な方法によりパッケージ(10)を製造することができる。さらに上述の第1実施例では樹脂モールド層(16)を形成する方法としてトランスファ・モールド法(多点成形法)を用いている。この方法は信頼性の高い樹脂封止ができるばかりでなく、モールドの強靭化、量産化が容易であるためにパッケージを自動的に製造できるという利点を有している。

なお上述の第1実施例において、第2A図に示す場合と同様にチップ収容部(19)及び外部電極部(17)(18)を設けた後に、基板(11)の上面を上述の$FeCl_3$系板を用いて低かにエッチングすることにより、第4A図に示すようにチップ収容部(19)及び外部電極部(17)(18)の下部の基板(11)にアンダーカット部(11a)～(11f)を形成し、次に第2B図～第2D図と同様な方法によつて第4B図に示すパッケージ(10)を完成させることができる。このように上記のエッチングによつてチップ収容部(19)及び外部電極部(17)(18)の下部に上記アンダーカット部(11a)～(11f)が形成されるので、これらの部分に樹脂が回り込んで突出部(20a)～(20f)が形成される。従つてこれらの突出部(20a)～(20f)によつて上記チップ収容部(19)及び上記外部電極部(17)(18)が下方から保持される形となるので、上記チップ収容部(19)及び上記外部電極部(17)(18)がパッケージ(10)の使用時において樹脂モールド層(16)から抜け出てしまうのを防止することができるという利点がある。さらにチップ収容部(19)及び外部電極部(17)(18)が樹脂モールド層(16)の下面から突出することなく形成されるので、これらのチップ収容部(19)及び外部電極部(17)(18)を全体薄くすることができるという利点もある。

第5A図～第5C図は本発明の第2実施例による半導体装置のパッケージの製造方法を説明するための工程図である。以下第5A図から工程順に説明する。

まず第5A図において、厚さうち〔a〕のCu製の基板(11)の上面に公知のフォトレジストを塗布した後に所定のパターニングを行う。次いでCuのみを選択的にエッチングするエッチング液、例えば既述の$FeCl_3$系板を用いて上記基板(11)の表面を低かにエッチングすることによつて、上記基板(11)の表面にチップ収容部位(11g)及び外部電極接続部位(11h)(11i)をそれぞれ形成する。上記フォトレジストを除去した後に第5B図において、第1実施例と同様に、上記チップ収容部位(11g)にハンダ層(15)を介してチップ(14)を収容した後、ワイヤボンディング法によつてこのチップ(14)と上記外部電極接続部位(11h)(11i)とをそれぞれAgの細線から成るワイヤ(21)で接続する。なお本実施例においては、後述の理由により、第1実施例で用いたワイヤよりも径の大きいワイヤを用いた。次に第1実施例と同様に樹脂モールド層(16)を上記基板(11)上に形成する。次に上記基板(11)を第1実施例と同様な方法でエッチング除去してパッケージ(10)を完成させる。上記エッチングにより露出されたワイヤ(21)の端部が外部電極部(17)(18)となり、また

ンダ(4)の下面が熱放散面(23a)となる。

上述のようにして完成されたパッケージ(20)をプリント基板上に実装する場合には、第1実施例と同様に、第5C図に示す上記外部電極部(11a)をプリント基板上の対応パターンに直接ハンダ付けして接続すればよい。このことから明らかなように、本実施例においてはワイヤ(5)の途部をそのまま外部電極部(11a)として用いるために、ワイヤ(5)の径を以下のように大きくするのが好ましい。なお熱放散面(23a)の機能は第1実施例と同様である。

上述の第2実施例のパッケージ(20)は、第1実施例のパッケージ(10)と異なつて、フオトレジスト工程及びエツチング工程によつて基板(1)に設けられた外部電極接続部位(11a)(11b)にワイヤ(5)を直接接続するようにしているので、第1実施例のパッケージ(10)におけるAu 層(12)(13)及びNi 層(13)を形成する必要がない。上記のフオトレジスト工程及びエツチング工程は第1実施例のパッケージ(10)で用いたメッキ工程よりもさらに簡便である。またこれらのフオトレジスト工程及びエツチング工程を用いることにより、Au 等の貴金属を用いる必要がなくなるという利点がある。

上述の第1実施例及び第2実施例においては、1個のチップをチップ載置部に載置してこれを樹脂モールドする場合につき述べたが、基板上に多数のチップ載置部を設け、それぞれのチップ載置部に同一のチップを載置して、これらのチップを一体に樹脂モールドした後に切断分離することにより、それぞれ1個のチップを有する同一のパッケージを多数個同時に作ることもできる。また種々のチップと、コンデンサや抵抗等の受動素子とを基板上に載置した後にこれらを一体に樹脂モールドすれば、種々の機能を有するパッケージを作ることができると共に、回路素子の実装度の高いパッケージを作ることができるという利点がある。

上述の第1実施例の基板の材料は選択エツチングが可能であればCu 等の他の金属であつてもよく、また第2実施例の基板の材料もFe 等の他の金属であつてもよい。第1実施例においてはさらに金属以外の材料、例えばポリイミドアミド系樹脂を用いることも可能である。この場合には以下のエツチング液としては、ヒドラジンとエチレンジアミンとの混合液を用いればよい。

発明の効果

本発明に係る半導体装置のパッケージの製造方法によれば、その動作時において半導体装置から発生する熱の放散性が良好でありかつ信頼性が高い小形のパッケージを、極めて簡便かつ安価な方法によつて自動的に製造することができる。

4 図面の簡単な説明

第1図は従来のプラスチックタイプのチップキャリアタイプパッケージの構造を示す断面図、第2A図～第2D図は本発明の第1実施例による半導体装置のパッケージの製造方法を説明するための工程図、第3図は上記第2A図に示す工程終了後の基板の平面図、第4A図及び第4B図は上記第1実施例の変形例を示す上記第2A図～第2D図と同様な図、第5A図～第5C図は本発明の第2実施例による半導体装置のパッケージの製造方法を説明するための工程図である。

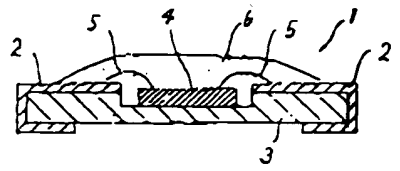
なお図面に用いた符号において、

(1)(2)(3)(4) …… パッケージ
(4) …… チップ
(5) …… ワイヤ
(1) …… 基板
(11a)(11b) …… 外部電極接続部位
(11) …… 外部電極部
(20) …… 樹脂モールド部

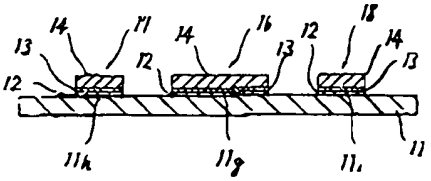
である。

代理人 土屋 勝
〃 名倉洋明
〃 杉浦俊貴

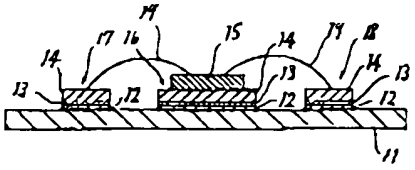
第１図



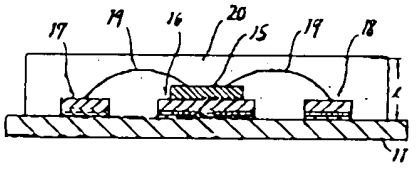
第２Ａ図



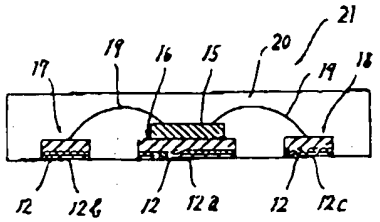
第２Ｂ図



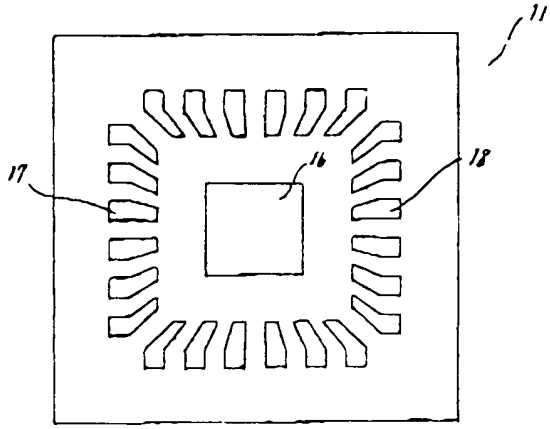
第２Ｃ図



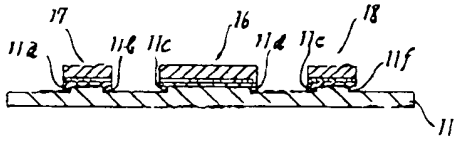
第２Ｄ図



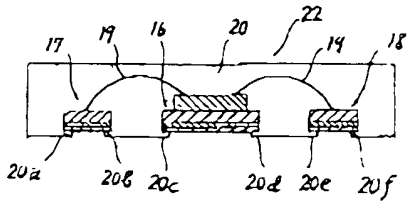
第３図



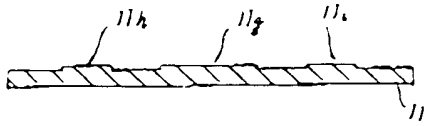
第４Ａ図



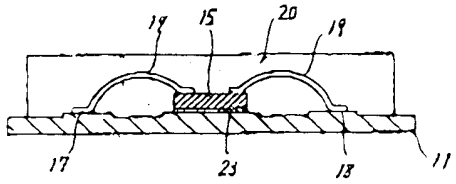
第４Ｂ図



第５Ａ図



第５Ｂ図



第５Ｃ図